PWM of Cascaded Multilevel Voltage Source Inverter using FPGA

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Abstract :Pulse Width Modulation has nowadays become an integral part of every electronics system. These techniques have been widely accepted and are researched extensively nowadays. It has found its application in large number of applications as a voltage controller. Its use in controlling output voltage of Inverter is the most frequently used application. There are basically two main techniques of PWM Generation- Analog technique and Digital Technique. This paper presents the development of Altium FPGA as a control circuit for generation of the digital pulse width modulation (DPWM) signal for the single-phase cascaded H-bridge multilevel inverter.

Index Terms- Cascaded H-bridge multilevel inverter, digital pulse width modulation (DPWM), field programmable gate array FPGA), Xilinx System Generator.

I. INTRODUCTION:

Multilevel inverters have grasped attention in the past few years as power converters in many applications. They are advantageous over the conventional two-level inverters because of the capability of reducing the lower order harmonic contents by increasing the number of levels. Many studies and research have been done for generation of modulating signals for multilevel inverters. Modulation signal generation methods for these inverters include staircase modulation, sine-triangle carrier modulation, space vector modulation etc. The various topological structures of the multilevel inverter suggestions must cope with the following points: 1) less number of switching devices, 2) capable of enduring high voltage and high power, and 3) lower switching frequency for the switching devices, . Cascaded H-bridge multilevel inverter is gaining faster development due to its topological and modularity significance. Digital PWM generation is considered as an alternate modulation technique in place of the conventional sinusoidal PWM using triangular carriers for the multilevel inverter operation that has the advantages of implementation simplicity and possibility to reduce harmonic distortions. Some methods use carrier disposition and others use phase shifting of the multiple carrier signals. Digital controllers, such as microprocessors, DSP, FPGA and application specific integrated circuits (ASIC) are gaining importance in the power electronics applications as they can easily implement DPWM, with better performance and at low cost . Therefore, digital control techniques are becoming more common solutions in modem power converters .In spite of the increasing popularity, the design of digitally controlled power converters is affected by several problems. Among them, software portability/re-usability is one strict concern. Though in most cases higher-level language is the programming choice and each program is strictly tied to the particular architecture, being I/O pins, peripherals and register settings are specific to each microprocessor. Therefore, any change in the digital processor, imposed by the introduction of new features or the need of better performance or the availability of cheaper components, requires a huge revision of the programming code, in order to comply with the new requirements. Such operations are time consuming, expensive and sometimes unsuccessful. Moreover, the expertise gained with a specific system could not be useful using different devices. In the last few years, the field programmable gate array (FPGA) circuits have become popular in the applications where high performance, low development, low production cost and fast time-to market are required. In fact, FPGA are functionally similar to standard ASICs but appear cost effective even in small-medium volume productions, thus allowing, the realization of powerful and cheap systems. Additionally, they almost eliminate the code portability issue as VHDL, the hardware description language, and several advanced development tools are almost device family independent. One emerging field which can obtain significant advantages by the use of FPGA is the multilevel converters. This is because the high number of switching components requires many output signals; needed to apply the modulation pattern to power devices. Most microcontrollers are not able to satisfy this demand. In fact, they can only generate few of them (generally six) because they are designed to control standard inverters. Multilevel converters often require complex control algorithms which cannot be implemented in real-time using standard low cost microcontrollers or DSP, but can be successfully implemented using hardware description languages and FPGA . modulation index. Xilinx ISE design suite14.2 is used to generate DPWM pattern and by the means Altium designer generated schematic diagrams and VHDL test bench programs the switching pattern is verified. The final design is converted in configuration data file and loaded into Altium nanoboard.

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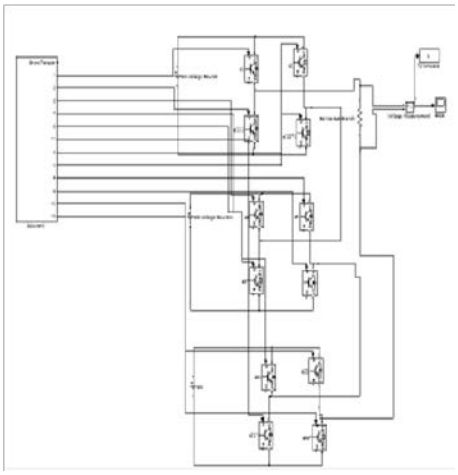
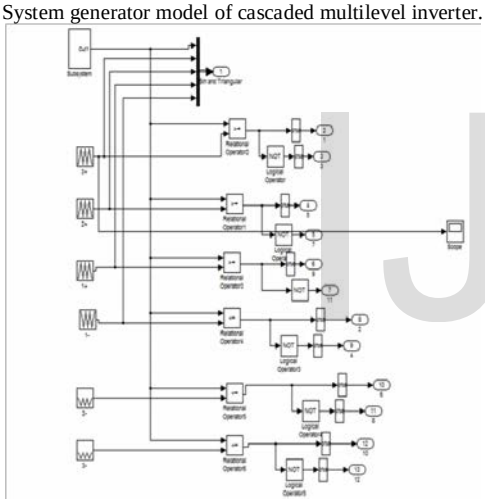
II. PWM Control of Inverter :

The application of PWM control in a Inverter (DC/AC) is shown in Fig. 2. The PWM control signal, VPWM in Fig. 2, is generated from PWM generator. This VPWM is logically ANDED with rectangular pulse waveform coming from pulse generator and is fed to power switches S1 and S3. The inverted rectangular waveform is logically ANDED with PWM waveform and is fed to power switches S2 and S4. Thus ON and OFF time of power switches are controlled by this PWM control signal to modulate input DC voltage to required AC voltage. The power switch is usually of MOSFET or IGBT. The size of Inverter depends on size of these power switches. Since frequency of operation is inversely dependent upon Inverter size

so we have to increase the switching frequency to reduce the Inverter size . So we have to look into the frequency aspect of PWM Generator used so that we get optimized size of Inverter by proper selection of frequency of PWM wave.



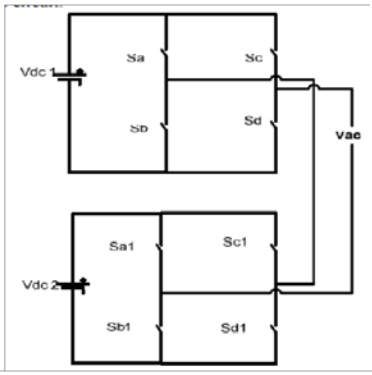
System generator model of cascaded multilevel inverter.



III. THE OPERATION OF CASCADED MULTILEVEL H-BRIDGE INVERTER

The cascaded H-bridge multilevel inverter circuit is shown in Fig. 5. The number of H-bridges required for an n-level inverter are N = (n-1)/2. Single-phase structure of the fivelevel cascaded H-bridge inverter is shown in Fig. 5. The output phase voltage is equal to the summation of the output of the each H-bridge module as below.

Vac = Vdc/2 + Vdc/2 + ……+ Vmh



S_{a1}	S_{b1}	S_{c1}	S_{d1}	S_a	S_b	S_c	S_d	V_{ac}
0	1	1	0	1	0	0	1	V_{dc}
0	1	1	0	1	0	1	0	$V_{dc}/2$
0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	$-V_{dc}/2$
1	0	0	1	0	1	1	0	$-V_{dc}$

Each module of the H-bridge has its own input voltage and consists of four switching power devices; Sa, Sb, Sc, and Sd. Each module of the cascaded multilevel inverter can produce three levels of the output voltage which is +V, 0 and –V. This is made possible by connecting the DC sources sequentially to the AC side via four power devices. For example cascaded H-bridge multilevel inverter with four modules of the Hbridge will produce nine levels of the output phase voltage; 4V, 3V, 2V, V, 0,-V,-2V,-3V and -4V). The cascaded H- bridge multilevel inverter has several advantages because of its simple and modular circuit configuration. Each of its modules is identical and incorporates both input and output circuitry. Besides, the cascaded H-bridge multilevel inverter requires the least number of components compared to other types of multilevel inverter. These features provide flexibility in extending cascaded Hbridge multilevel inverter to higher number of levels without modification on the circuit itself. The switching signal and the output voltage are shown in Table I.

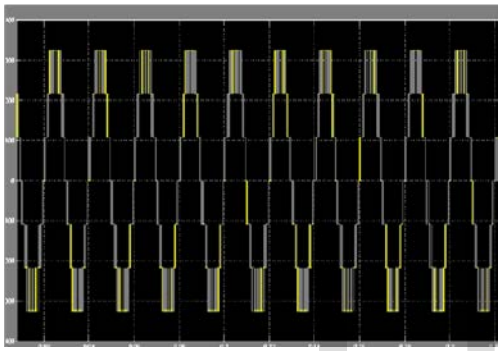
IV. FPGA BASED CONTROL ALGORITHM:

The FPGA controller is designed as a card to be plugged into a personal computer, which uses a peripheral component interconnect (PCI) bus to communicate with the microcomputer in which a Visual Basic interface is used to input and adjust the control schemes and parameters. The FPGA controller is designed as a card to be plugged into a personal computer, which uses a peripheral component interconnect (PCI) bus to communicate with the microcomputer in which a Visual Basic interface is used to input and adjust the control schemes and parameters.

V. RESULTS

The proposed five-level cascaded multilevel PWM single phase inverter is simulated by usingMATLAB/Simulink®, XILINX® 14.2 simulation software and Altium designer software. The system is tested and simulated with resistive and inductive loads. The VHDL

schematic entity is developed for DPWM generation using Altium designer board and the result is displayed on digital storage oscilloscope. The six different levels of the carrier signals (such as saw tooth signals) are compared with the sinusoidal (reference signal) as shown in figure. 7. Each saw tooth signal is of the same amplitude and same frequency of 1 kHz that is generated from the up-counter. The 6.0 V amplitude and 50 Hz frequency sine wave is produced by up-counter along with ROM devices. The output voltage waveform of five-level cascaded H-bridge inverter has been simulated and shown in figure 8.Eight DPWM gating signals for firing the cascaded h-bridge inverter across the scope is shown in figure 9.The system generated VHDL code and its test bench is simulated for the accurate results of the DPWM signals in Xilinx platform, shown in figure .Finally the generated HDL code is dumped on Altium nanoboard and the switching pulses as simulated is verified on digital storage oscilloscope as shown in figure 11.The complete hardware co simulation experimental setup for generation of DPWM .



Five-level cascaded multilevel inverter output voltage.

VI. CONCLUSION

The Altium based FPGA digital control switching patterns are adopted and applied to the cascaded multilevel inverter switches to generate multilevel output voltages. The FPGA reduces complexity, increases speed and adds flexible in the design of the control circuit for hardware implementation. It can efficiently extend the range of modulation index which facilitates a better quality output voltage with minimal distortion. The experimental, simulation and hardware implementation results demonstrate the improved quality voltage waveform shapes at the output of the inverter.

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